Notice of Allowability	Application No.	Applicant(s)	
	09/734,856	TAKEUCHI ET AL.	
	Examiner	Art Unit	
	Jason M. Perilla	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendement filed December 14, 2005*.

2. ☒ The allowed claim(s) is/are *1, 3-7, and 10 renumbered respectively as claims 1-7*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20060306* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. Claims 1, 3-7, and 10 are pending in the instant application.

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Dexter T. Chang on March 3, 2006.

The application has been amended as follows wherein the following versions of claims 1, 4-6, and 10 are replace all prior versions in their entirety:

1. An apparatus, comprising:

a plurality of received-signal registers which receive and store therein a plurality of respective received-signal sequences;

a first selector which selects one of the received signal sequences stored in said received-signal registers;

at least one code register which stores therein a de-spreading-code sequence;

a multiplication circuit which multiplies the selected one of the received-signal sequences by the de-spreading-code sequence; and

a summation circuit which obtains a sum of results of the multiplication to obtain a correlation between the selected one of the received-signal sequences and the de-spreading-code sequence;

wherein said at least one code register includes a first code register storing a first de-spreading code and a second code register storing a second de-spreading code, wherein the pattern of the first de-spreading code and the pattern of the second de-spreading code are different, and said apparatus further comprising a second selector which selects one of said first code register and said second code register to select and supply the de-spreading-code sequence to the multiplication circuit, and

wherein while the correlation between the selected ~~one of the~~ received signal sequences of the selected received-signal register and the selected one of the de-spreading-code patterns is being obtained, ~~another one of the~~ a received signal sequences ~~is written to said~~ of another received-signal registers of the plurality of received signal registers is replaced.

4. An apparatus, comprising:

a plurality of received-signal registers which receive and store therein a plurality of respective received-signal sequences;

a selector which selects one of the received signal sequences stored in said received-signal registers;

at least one code register which stores therein a de-spreading-code sequence;

a multiplication circuit which multiplies the selected one of the received-signal sequences by the de-spreading-code sequence;

a summation circuit which obtains a sum of results of the multiplication to obtain a correlation between the selected one of the received-signal sequences and the de-spreading-code sequence

a delay-profile-holding unit which generates a delay profile based on correlations obtained by the summation circuit;

a path-timing-detection circuit which detect a path timing by detecting a peak of the delay profile;

a first sequence-order-control circuit which converts a single received-signal sequence arranged in a first order into k received-signal sequences arranged in a second order where k is an integer more than one, the k received-signal sequences being supplied to said plurality of received-signal registers; and

a second sequence-order-control circuit which converts the delay profile from one corresponding to the second order to one corresponding to the first order.

5. The apparatus as claimed in claim 4, wherein the single received-signal sequence has a spreading factor m, where m is an integer, and an over-sample ratio that is equal to k, and each of the k received-signal sequences has m samples therein, and wherein each of said plurality of received-signal registers has m stages.

6. An apparatus, comprising:

a plurality of received-signal registers which receive and store therein a plurality of respective received-signal sequences;

a first selector which selects one of the received signal sequences stored in said received-signal registers;

at least one code register which stores therein a de-spreading-code sequence;

a multiplication circuit which multiplies the selected one of the received-signal sequences by the de-spreading-code sequence;

a summation circuit which obtains a sum of results of the multiplication to obtain a correlation between the selected one of the received-signal sequences and the de-spreading-code sequence;

N received-signal-holding units which hold therein N received-signal sequences, where N is an integer;

a second selector which successively selects one of said N received-signal-holding units, and supplies the successively selected one of the N received-signal sequences to said plurality of received-signal registers at a speed N times faster than sampling speed of the N received-signal sequences;

N delay-profile-holding units which generate N delay profiles corresponding to the N received-signal sequences based on correlations obtained by the summation circuit;

a third selector which successively selects one of said N delay-profile-holding units, and supplies the successively selected one of the N delay profiles; and

a path-timing-detection circuit which detect a path timing by detecting a peak of the successively selected one of the N delay profiles.

10. An apparatus for obtaining a correlation wherein a correlation calculating unit calculates the correlation while shifting, relative to a de-spreading code, a phase of a ~~received~~ signal spread by a spreading code, comprising:

a first shift register configured to store a first received signal;

a second shift register configured to store a second received signal;

a selector unit configured to selectively output one of the first received signal and the second received signal; and

a control unit configured to cause said selector unit to output the first received signal and to cause the correlation calculating unit to calculate a correlation with respect to the first received signal, followed by causing said selector unit to output the second received signal and by causing the correlation calculating unit to calculate a correlation with respect to the second received signal,

wherein ~~a signal obtained by oversampling~~ a received signal is oversampled and ~~is~~ picked every few samples to generate two or more sequences, and wherein the first received signal is a first one of the two or more sequences and the second received signal is a second one

of the two or more sequences, the correlation calculations of the first received signal and the second received signal being preformed by use of a common de-spreading code, and

wherein said second shift register shifts the second received signal to set the second received signal to a predetermined phase while correlation calculation is being performed for the first received signal.

Claims 1, 3-7, and 10 are renumbered respectively as claims 1-7.

Allowable Subject Matter

3. Claims 1, 3-7, and 10 renumbered respectively as claims 1-7 are allowed.

4. Claims 1, 3-7, and 10 renumbered respectively as claims 1-7 are allowed because the prior art of record does not disclose or obviate the claimed apparatus wherein one of two signal registers holding received signals is selected for correlation and the other one (un-selected) of the two signal registers is concurrently loaded with a new portion of a received signal. Furthermore, the prior art of record does not disclose or obviate the claimed apparatus wherein the un-selected one of the two signal registers shifts its received signal while the selected register's signal is being correlated.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M. Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
March 3, 2006

jmp

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER